REMARKS

In accordance with the foregoing, claims 1, 3, 4, 5, 7, 8, 11, 12, and 15-17 have been amended.

Claims 1-17 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 103:

On page 2 of the Office Action, claims 1 and 5 are rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,067,611 to Carpenter ("Carpenter") and U.S. Patent No. 6,263,405 to Irie ("Irie").

As correctly noted by the Office Action, Carpenter fails to teach or suggest "holding data preread from a system module, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1. Thus, Irie is relied upon as teaching such claimed features.

However, Irie merely proposes (a) a queuing buffer (FIFO) within a crossbar unit, and (b1) prereading from a memory and queuing within a memory board or, (b2) prereading from a memory and transferring the preread data to a processor board for queuing within the processor board (by the buffer). See FIGS. 1 and 10 of Irie.

But according to an aspect of the present invention, for instance, independent claim 1 uses (A) a buffer (data buffer which can change the transfer sequence) within a crossbar module, and (B) prereads and transfers the preread data from a system module to the crossbar module (by lowering the priority if necessary) for queuing within the crossbar module.

The features (A) and (B) of the present invention are completely different from the features (a) and (b1) or (b2) of Irie.

With regard to the prereading, Irie describes the buffering within the memory board and a possibility of transferring the preread data to the processor board. (see column 1B, lines 25-49). Although Irie teaches a crossbar unit, Irie does not teach or even suggest queuing within the crossbar unit.

Applicants respectfully assert that, in Irie, it is always the memory board that receives the transfer enable/disable (permit/prohibit), **and not** the crossbar unit 40.

Further, Irie generally describes that a cache access controller 21 judges that the cache has missed and a transaction send circuit 22 sends a data read transaction as a coherent read

request to a crossbar unit 40. See column 6, line 49, to column 7, line 7. The crossbar unit 40 multicasts **this** data (i.e., the data read transaction from the transaction send circuit 22) to **all** the processor boards. Emphasis added. In contrast, independent claim 1 recites, "holding data preread **from one of** the system modules, **other than the arbitrary system module**, in **a buffer within the crossbar module**." Irie does not teach or suggest that the data read transaction is from one of the system modules, other than the arbitrary system module and does not teach or suggest that the data read transaction is held in a buffer within the crossbar unit 40. Rather, all the processor boards receive the data. There is no teaching or suggestion of a buffer within the crossbar unit 40 holding data preread.

In addition, Irie describes the buffering within the memory board and the possibility of transferring the preread data to the processor board (See column 18, lines 25-49 of Irie). Accordingly, rather than holding data preread from the system module, the crossbar unit 40 transfers the data transaction to the processor board 10-0 which issued the coherent read request (step 909).

In addition, Irie fails to teach or suggest, "transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module," as recited in independent claim 1.

As may be seen from FIG. 6 of Irie showing the crossbar unit, the data queue (INQ) has a FIFO (in-order) structure for each port, and it is clear that Irie cannot lower the priority by reversing the order for the memory preread.

But in the present invention, the priority may be lowered in the crossbar module because the priority order control maintains the cache coherency.

Therefore, according to the present invention, it is possible to freely carry out the queuing within the processor, the system module and the crossbar module. In contrast, Irie can carry out the queuing only within the memory board. Irie does not teach or suggest enabling the queuing location to be selected dynamically as done in the present invention. The present invention enables an efficient data transfer, because the queuing location can be selected dynamically by assigning an arbitrary priority order.

Accordingly, a person of ordinary skill in the art would not have arrived to the recitations of the present invention in view of Carpenter and Irie, combined.

The arguments presented above are incorporated herein to support the patentability of

claim 5 over Carpenter and Irie.

On page 5 of the Office Action, claims 2 and 6 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,055,650 to Christie ("Christie").

The arguments presented above are incorporated herein to support the patentability of claims 2/1 and 6/5 over Carpenter and Irie.

Christie generally describes detecting a phase change in a program being executed and reducing a number of prefetching operations. A prefetch unit is configured to selectively prefetch in response to the detected phase changes. See column 2, lines 36-67, and column 5, line 51, to column 6, line 35 of Christie. However, similarly to Carpenter and Irie, Christie fails to teach or suggest, "responsive to a read request from a processor within an arbitrary system module, holding data preread from one of the system modules, other than the arbitrary system module, in a buffer within the crossbar module," as recited in independent claim 1.

In addition, Christie fails to broach the features recited in independent claim 1 reciting, "transferring the preread data from the system module, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module." Thus, Carpenter, Irie, and Christie, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

The arguments presented above are incorporated herein to support the patentability of claim 5 over Carpenter, Irie, and Christie.

It is respectfully requested that independent claims 1 and 5 and related dependent claims be allowed.

On page 6 of the Office Action, claims 4, 8, and 12-15 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 5,761,452 to Hooks ("Hooks").

The arguments presented above are incorporated herein to support the patentability of claims 4/1, 12/1, 13/1, 8/5, 14/5, and 15/5 over Carpenter and Irie.

Hooks generally describes a bus arbiter method assigning a priority to a requesting master when a pre-fetch signal is or is not asserted. See column 5, lines 18-25 of Hooks.

In particular, Hook provides a bus arbiter configured such that when a first bus master

asserts its REQ signal and its SP signal and the second bus master asserts its REQ signal, the bus arbiter assigns higher priority to the second bus master in response to the SP signal. See abstract. Specifically, if a particular requesting master asserts its request signal REQ# and asserts its speculative pre-fetch signal SP#, state machine 50 assigns a lower priority to the requesting master in comparison to a priority it would have received if the speculative pre-fetch indicator signal had not been asserted. See column 5, lines 17-25. That is, the priority for a particular bus master's request is lowered if the request is accompanied by a corresponding speculative pre-fetch signal.

Hook provides an opposite embodiment to the one provided in the present application. In Hook, the priority of the requesting master is lowered, however, in the present invention the data preread is lowered in priority compared to the priority of the normal data transfer. Specifically, the preread data from the system module is transferred, other than the arbitrary system module, to the buffer within the crossbar module, "with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module," as recited in independent claim 1.

Thus, Carpenter, Irie, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 1.

The arguments presented above are incorporated herein to support the patentability of claim 5 over Carpenter, Irie, and Hooks. It is respectfully requested that independent claims 1 and 5 and related dependent claims be allowed.

On page 9 of the Office Action, claims 3 and 7 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Christie, and Hooks.

The arguments presented above are incorporated herein to support the patentability of claims 3/1 and 7/5 over Carpenter, Irie, Christie, and Hooks. It is respectfully requested that independent claims 1 and 5 and related dependent claims be allowed.

On page 10 of the Office Action, claim 9 is rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,341,337 to Pong ("Pong").

The arguments presented above are incorporated herein to support the patentability of claim 9/5 over Carpenter and Irie.

Pong generally describes a cache controller 208 performing a lookup in the tag memory for the requested address (step 302). See FIG. 6 and column 7, lines 25-60. If the address is not in the tag memory (step 304-N), no further processing is performed. If the address is found

in the tag memory (step 304-Y), the state of the tag is analyzed (step 306). Simultaneously with the action of the cache controller 208, the bus watcher 212 determines whether the snooped address corresponds to the shared memory stored in the node's main memory unit 210 (step 312). However, similarly to Carpenter and Irie, Pong is silent as to teaching or suggesting, "said crossbar module including a buffer which holds data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module," as recited in independent claim 5.

In addition, Pong is silent as to teaching or suggesting "said one of the system modules transferring the preread data from the one of the system modules, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module," as recited in independent claim 5. The cited reference says nothing about changing the priority of the data as recited in independent claim 5.

Thus, Carpenter, Irie, and Pong, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 5. It is respectfully requested that independent claim 5 and related dependent claims be allowed.

On page 10 of the Office Action, claims 10-11 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, and U.S. Patent No. 6,263,415 to Venkitakrishnan ("Venkitakrishnan").

The arguments presented above are incorporated herein to support the patentability of claim 10/5 over Carpenter and Irie.

Venkitakrishnan generally describes a backup redundant routing system providing a crossbar switch using a plurality of chips. Nodes 200, 300, 400, and 500 are connected to crossbar switches 600 and 700, providing a flexible structure that allows dynamic programming of the data routing and enable support of different network architectures. See column 3, lines 7-38 of Venkitakrishnan. However, similarly to Carpenter and Irie, Venkitakrishnan fails to teach or suggest, "said crossbar module including a buffer which holds data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module, wherein the data preread is data at a location that is close to the processor that made the read request," as recited in independent claims 5 and 11.

Venkitakrishnan is silent as to changing the priority of the data. Specifically, Venkitakrishnan is silent as to teaching or suggesting that "said one of the system modules

transferring the preread data from the one of the system modules, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module," as recited in independent claims 5 and 11.

Thus, Carpenter, Irie, and Venkitakrishnan, individually or combined, fail to teach or suggest all the claimed features recited in independent claims 5 and 11.

It is respectfully requested that independent claims 5 and 11 and related dependent claims be allowed.

On page 13 of the Office Action, claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Carpenter, Irie, Venkitakrishnan, and Hooks.

The arguments presented above are incorporated herein to support the patentability of claim 16/11 and 17/11 over Carpenter, Irie, and Venkitakrishnan.

Hooks, similarly to Venkitakrishnan, Carpenter, and Irie, fails to teach or suggest, "said crossbar module including a buffer which holds the data preread from one of the system modules, other than an arbitrary system module, responsive to a read request from a processor within the arbitrary system module," as recited in independent claim 11.

As previously set forth, Hooks provides an opposite embodiment to the one provided in the present application. In Hooks, the priority of the requesting master is lowered, however, in the present invention the data preread is lowered in priority compared to the priority of the normal data transfer.

Hooks fails to teach or suggest, "said one of the system modules transferring the preread data from the one of the system modules, other than the arbitrary system module, to the buffer within the crossbar module, with a priority lower than a priority of a normal data transfer between the system modules and the crossbar module," as recited in independent claim 11.

Thus, Carpenter, Irie, Venkitakrishnan, and Hooks, individually or combined, fail to teach or suggest all the claimed features recited in independent claim 11. It is respectfully requested that independent claim 11 and related dependent claims be allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding

objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: ____August 23, 2004____ By: _____

Alicia M. Choi
Registration No. 46,621

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501